UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,535	04/08/2004	Mehmet Aslan	50019.0225USU1	8319

23552 7590 04/05/2006

MERCHANT & GOULD PC
P.O. BOX 2903
MINNEAPOLIS, MN 55402-0903

EXAMINER	
VERBITSKY, GAIL KAPLAN	
ART UNIT	PAPER NUMBER
2859	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/820,535	ASLAN ET AL.
	Examiner	Art Unit
	Gail Verbitsky	2859

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4, 8-9, 13-16, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tuthill (U.S. 5982221).

Tuthill discloses in Fig. 2 a device in the field of applicant's endeavor comprising a dual diode temperature sensor (transistors 66 and 68) collocated on a common substrate wherein emitters (first electrodes) of the transistors are connected to first terminal C1 and second terminal C2 respectively, bases (second electrodes) are biased with AGND (biasing circuit) by means of a third terminal, wherein the first electrodes have polarity opposite to the second electrodes. The device further comprises a differential ADC part of which is a differential amplifier 78. All the terminals are used to measure temperature related voltage.

Tuthill does not explicitly teach to collocate the measuring circuit (differential ADC) onto a second substrate.

Beer discloses a device in the field of applicant's endeavor wherein a temperature measuring circuit is collocated on a second substrate apart from a first substrate (entire col. 3).

Therefore, it would have been obvious to one of ordinary skills in the art at the time the invention was made to modify the device, disclosed by Tuthill, so as to collocate the temperature measuring circuit on a second substrate apart from the first substrate, in order to make the second substrate usable with a plurality of first substrates in a multiplexing circuit, so as to minimize manufacturing costs.

3. Claims 1, 3, 5, 8, 10, 12, 14, 15, 17, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunst (U.S. 6008685) in view of Tuthill.

Kunst discloses in Fig. 6 a device in the field of applicant's endeavor and teaches that a measurement circuit including bias can be collocated on a single/ separate (second) substrate 600. Kunst also teaches that diodes can be npn or pnp transistors or diodes, inherently, having anodes and cathodes (first and second electrodes respectively. Kunst also teaches a first terminal connected to a first electrode (cathode) of a diode 650-1, a second terminal connected to a first electrode (cathode) of a second diode 650-2, and a third electrode/ bias circuit) biasing (grounding) second (anodes) electrodes of the diodes.

Kunst does not explicitly teach that the dual diode is located on a common (first) substrate, as stated in claim 1, and a differential ADC, as stated in claim 14.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device disclosed by the Prior art, so as to have more than one (two) sensing diode, as taught by Kunst, so as to solve a problem of two current sources mismatching, as already suggested by Kunst.

Tuthill discloses in Fig. 2 a device in the field of applicant's endeavor comprising a dual diode temperature sensor (transistors 66 and 68) collocated on a common substrate wherein emitters (first electrodes) of the transistors are connected to first terminal C1 and second terminal C2 respectively, bases (second electrodes) are biased with AGND (biasing circuit) by means of a third terminal, wherein the first electrodes have polarity opposite to the second electrodes. The device further comprises a differential ADC part of which is a differential amplifier 78. All the terminals are used to measure temperature related voltage.

Therefore, it would have been obvious to one of ordinary skills in the art at the time the invention was made to modify the device, disclosed by Kunst, so as to collocate the dual diodes onto the same common substrate, as taught by Tuthill, so as to enable the device to accurately measure a temperature of the substrate, since substrates, chips, modules, IC tend to overheat, therefore, their temperature should be accurately measured and controlled.

Therefore, it would have been obvious to one of ordinary skills in the art at the time the invention was made to modify the device, disclosed by Kunst, so as to have a differential ADC, as taught by Tuthill, so as to enable the device to calculate the output voltage signal from both, first and second voltages and to convert the output voltage signal in a digital form so as to make it readable by a compute, as it is very well known in modern technology.

The method steps will be met during the normal operation of the device stated above.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kunst, Tuthill, as applied to claims 1, 3, 5, 8, 10, 12, 14, 15, 17, 19 above, and further in view of Shih (U.S. 20030133491 filing date 01/04/2002).

Kunst and Tuthill disclose the device as stated above.

They do not explicitly teach the limitations of claim 7.

Shih discloses in Fig. 1 a device in the field of applicant's endeavor comprising a dual diode system (D1, D2). In calibration mode, Shih teaches to provide a first current through both diodes, while, in the run (operation) mode, Shih teaches to provide a second current only to the first diode, inherently using, only first terminal for two currents.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device, disclosed by Kunst and Tuthill, so as to use only one diode (first terminal) during measurement mode, while the second terminal is used for calibration mode, as already, suggested by Shih, because, it is very well known in the art that, in order to provide accurate measurements, diodes should first be calibrated.

5. Claims 1, 6, 8, 13, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (U.S. 5660474) in view of Kunst and Beer.

Kurihara discloses a device in the field of applicant's endeavor comprising a dual diode (transistor) system collocated in the same location and comprising a first transistor 10 having a first electrode (collector) connected to a first terminal, a second transistor 11 has a first electrode 9collector) connected to a second terminal, the device

also has a third terminal connected to a second electrode (base) of each transistor and a bias circuit biasing the third terminal. The device also has a temperature measurement circuit. An output voltage is measured and inherently, the measurement involves using first, second and third terminals.

Kurihara does not explicitly teach to position/ collocate the diodes on a first substrate, and the temperature measurement circuit on a second diode.

Kunst discloses in Fig. 6 a device in the field of applicant's endeavor and teaches that a measurement circuit including bias can be collocated on a single/ separate substrate 600. Kunst also teaches that diodes can be npn or pnp transistors or diodes, inherently, having anodes and cathodes (first and second electrodes respectively

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device disclosed by the Kurihara, so as to have more than one (two) sensing diode, as taught by Kunst, so as to solve a problem of two current sources mismatching, as already suggested by Kunst.

Beer discloses a device in the field of applicant's endeavor wherein a temperature measuring circuit is collocated on a second substrate apart from a first substrate (entire col. 3).

Therefore, it would have been obvious to one of ordinary skills in the art at the time the invention was made to modify the device, disclosed by Kurihara, so as to collocate the temperature measuring circuit on a second substrate apart from the first substrate, in order to make the second substrate usable with a plurality of first substrates in a multiplexing circuit, so as to minimize manufacturing costs.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3, 4, 8, 10, 11, 13, 15, 17, 18, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Aslan et al. (U.S. 6149299) [hereinafter Aslan].

Aslan discloses in Fig. 6 a device in the field of applicant's endeavor comprising a dual diode sensor collocated/ formed on a first common substrate B, a temperature measuring circuit formed on a second substrate A. the device further comprises a first terminal connected to a cathode/ first electrode of the diode J1, a second terminal connected to a cathode/ first electrode of the diode J2. The device also has a third terminal connected to anodes/ second electrodes of the diodes, and grounding them. The bias circuit is located on the first substrate. The voltage measurements are done by using at least one first or second terminal. The measuring circuit is configured to measure voltage using at least one (both) first and second terminals.

Response to Arguments

8. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art cited in the PTO-892 and not mentioned above disclose related devices and methods.

Kurihara (U.S. 5660474) discloses in Fig. 1 a device in the field of applicant's endeavor comprising two temperature measuring transistors 10 and 11, whose second electrodes (base) is biased with a bias voltage by means of third terminals, first electrodes of transistors 10 and 11 are connected to first and second terminals respectively.

Lien (U.S. 6019508) discloses a device in the field of applicant's endeavor comprising first and second transistors 17-1 and 17-n

Davidson et al (U.S. 5639163) discloses a device in the filed of applicant's endeavor wherein a temperature measuring circuit comprising biasing circuit (Vp), differential amplifier and ADC are located outside the first substrate/ chip.

Barton (U.S. 3181364) discloses in Fig. 1 a temperature sensing circuit comprising a dual diode system wherein first diode T1 has a first electrode (collector) and a second electrode (base) wherein the first electrode of T1 has the same polarity as a first electrode of a second diode T2, and the base of T1 has the same polarity as a base of T2. The device also has a first terminal through CRI is coupled to the first electrode of T1; a second terminal through CR2 is coupled to the first electrode of T2. A third terminals is coupled (biasing) by means of a bias circuit/ bias diode D1 the second electrodes (bases) of T1 and T2. The transistors are exposed to the same temperature. It is inherent, that the first polarity and the second polarity are different and opposite to each other. It is, inherent, that when voltage/ current is being measured, the third terminal must be used.

Grannes et al. (U.S. 7018095) discloses a device in the field of applicant's endeavor wherein a temperature measuring circuit is collocated on a second substrate and is configured to perform voltage measurements using at least first and second terminals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gail Verbitsky whose telephone number is 571/ 272-2253. The examiner can normally be reached on 7:30 to 4:00 ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571/ 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GKV

Gail Verbitsky
Primary Patent Examiner, TC 2800

March 30, 2006